C-based HLS Coding for Software Designers

Course Description

C-based coding is increasingly used for the modeling and high-level synthesis of hardware components. This course provides software engineers with sufficient knowledge of FPGA hardware to efficiently code for high-level synthesis. Learn the high-level synthesis best practices, methodology, and subtleties of C-based coding for hardware modeling, synthesis, and verification.

Level: DSP 3

Training Duration: 1 Day

Who Should Attend?

Software engineers looking to utilize high-level synthesis

Prerequisites:

- C, C++, or SystemC knowledge
- Software design experience

Software Tools:

- Vivado™ System Edition 2012.2

Hardware:

- Architecture: Zynq™-7000 All Programmable SoC and 7 series FPGAs*
- Demo board: None

Skills Gained: After completing this training, you will be able to:

- Describe the difference between software programming and hardware design
- Identify the fundamental principles of hardware design
- Model and simulate hardware components using C
- Code hardware components in C for high-level synthesis

Course Outline

1. Introduction to Hardware Design for Software Designers
Lab 1: Analyze a Simple Top-Level Hardware Design

2. C-based Algorithmic Coding for Hardware
Lab 2: High-Level Synthesis of a C Model

3. C-based Test Bench Coding
Lab 3: Creating a C-based Test Bench

Lab Description

Lab 1: Analyze a Simple Top-Level Hardware Design – Analyze a top-level, two-frequency pulse width modulator (PWM) hardware system. Identify and analyze hardware design components, parallel flow, and control.

Lab 2: High-Level Synthesis of C Model – Use various techniques and directives in Vivado HLS to improve design performance. The design under consideration accepts an image in a (custom) RGB format, converts it to the Y'UV color space, and applies a filter to the Y'UV image and converts it back to RGB.

Lab 3: Creating a C-based Test Bench – Develop a verification environment used for testing a C-based design and verification in Vivado HLS. The design under consideration is the same design used in the previous lab, a Y'UV filter.