

USB 3.0 Architecture

Duration: 2 Days

Course Overview:

The purpose of this course is to provide the student with the theoretical knowledge required for defining and implementing systems based on USB versions 2 & 3.

The course begins with basic concepts and then fully describes in detail USB Architecture (USB2.0 & USB 3.0). The material is fully up-to-date and supports the latest version of the international specification.

The course covers partially also OTG, UTMI, LPM, EHCI and HSIC.

During the course there are many examples which cover all aspects of USB specification.

Who should attend?

This course is designed for Project Managers, Software and Hardware Engineers who design and implement USB 2 & 3.

Objectives:

By the end of this course, the student will:

Be able to define the required performance and define USB Descriptors

Be able to design and debug USB devices (HW & SW).

Course Content:

Part I – Background & Fundamentals

- USB Motivation
- Bus Topology
- Endpoints
- USB 2.0 Data Flow (Bulk, Isochronous, Interrupt, Control)
- USB 3.0 Basic Concept (Mechanical, Power Management, Packet Routing)
- Super Speed Layers

Part II – USB 3.0 Architecture

- Physical Layer
- Protocol Layer
- Link Layer

Part III – Power Management

- U0
- U1
- U2
- U3
- System Exit Latency
- Self & Bus Power Device

Part IV – Descriptors

- Device States
- Device Class
- Descriptor Tree
- Device Descriptor
- Control Descriptor
- Interface Descriptor
- Endpoint Descriptor
- Endpoint Companion Descriptor
- BOS

Part V – Control Transfer

- USB 2.0 Control Transfer
- USB 3.0 Control Transfer
- Setup – Standard Request Code

Part VI – USB Hub

- Hub Architecture
- Hub Routing & Signalling
- Hub Descriptors
- Port Status

Part VII - Examples

- Configuration Device
- HID Class
- Mass Storage Class
- USB 3.0 Tracer Plot

Part VIII – Supplement Specifications

- OTG
- HSIC
- UTMI
- xHCI